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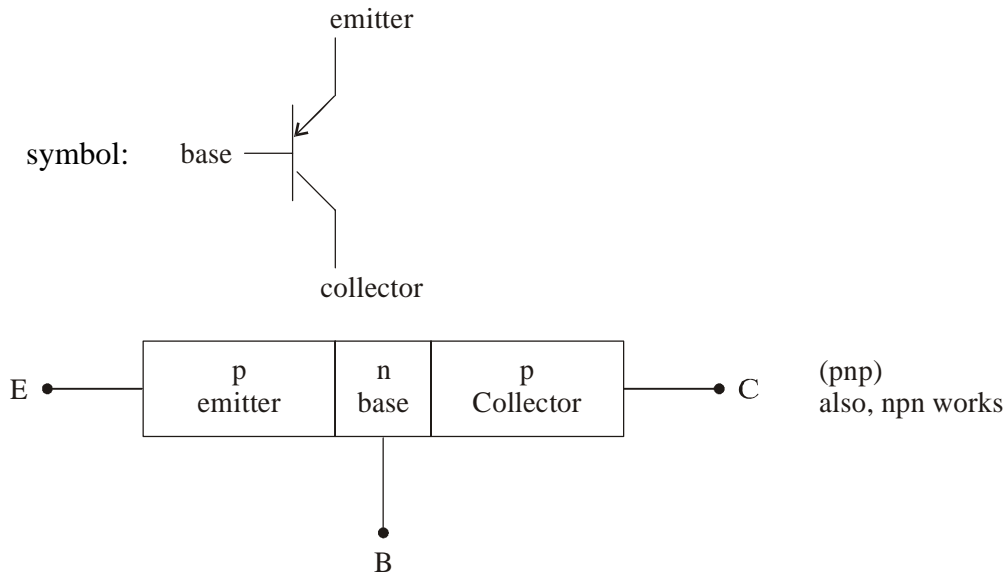
**Advice:**

Today: lec 5 JFET I  
lec 6 TH Feb 8  
lec 7 TH Feb 15  
lec 8 TH Feb 22

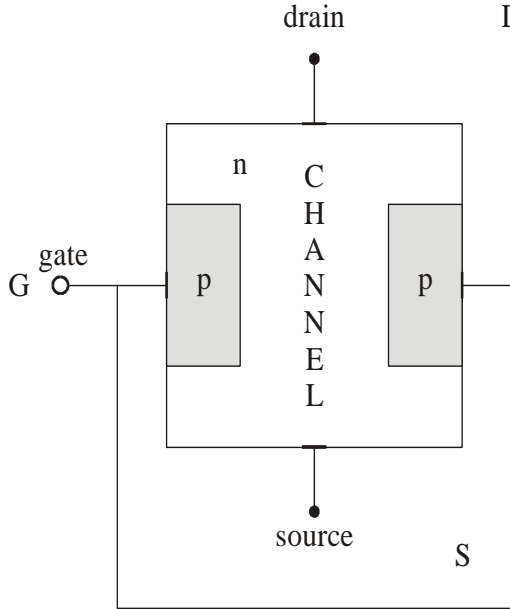
solutions posted  
hand in late labs

**Instruments & Devices**

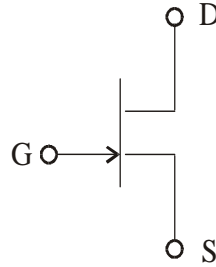
- Now move to 3-terminal semiconductor devices. Why? – Enormously useful because the use of a control signal (voltage or current, depending on the device) between 2 terminals is used to control current in the third terminal.
- Two major device varieties:  
bipolar junction transistor BJT



- Second is a field effect transistor (FET)
  - a number of varieties of these, simplest is junction FET or JFET

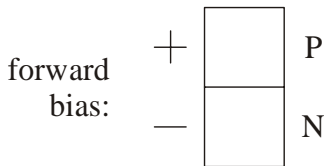


n-channel JFET

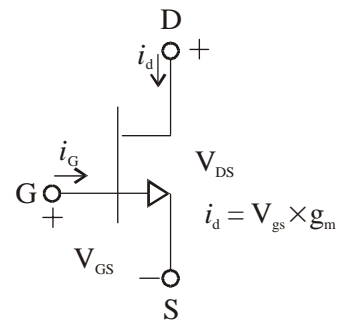
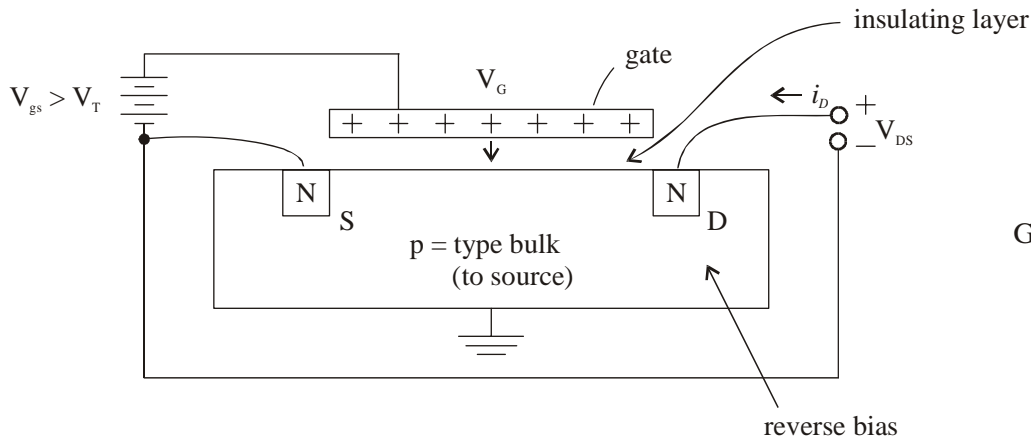


gate pinches off current flow in channel (see Sedra)

More important: MOSFET (CMOS is basis of much circuitry eg. Your laptop)



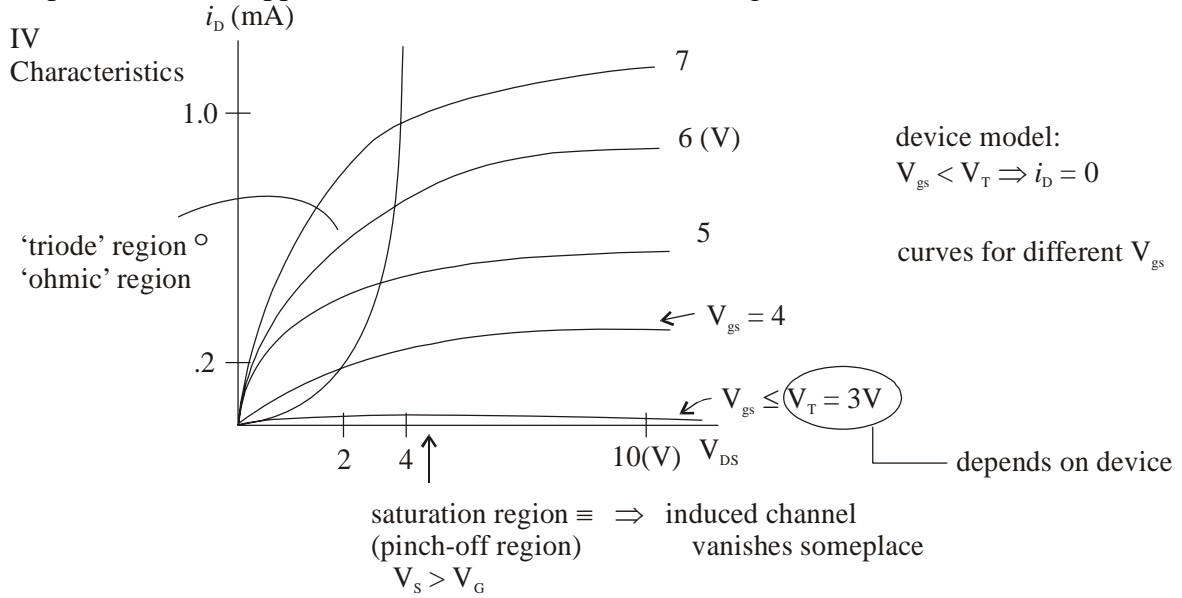
Metal-Oxide-Semiconductor Field Effect Transistor (section 9.2)  
MOSFET



P-N junctions = diodes, one is back biased (for any  $V_{DS}$ ), nothing happens  
 Convert region near surface from p to n via field. (electrons drawn from source region)  
 Gate insulated: almost no input current. (Voltage operated device)  
 Enhancement mode device – charge carriers added to channel ( $V_g = 0 \Rightarrow$  no conduction)

(depletion mode – opposite)

[source = source of charge carriers]



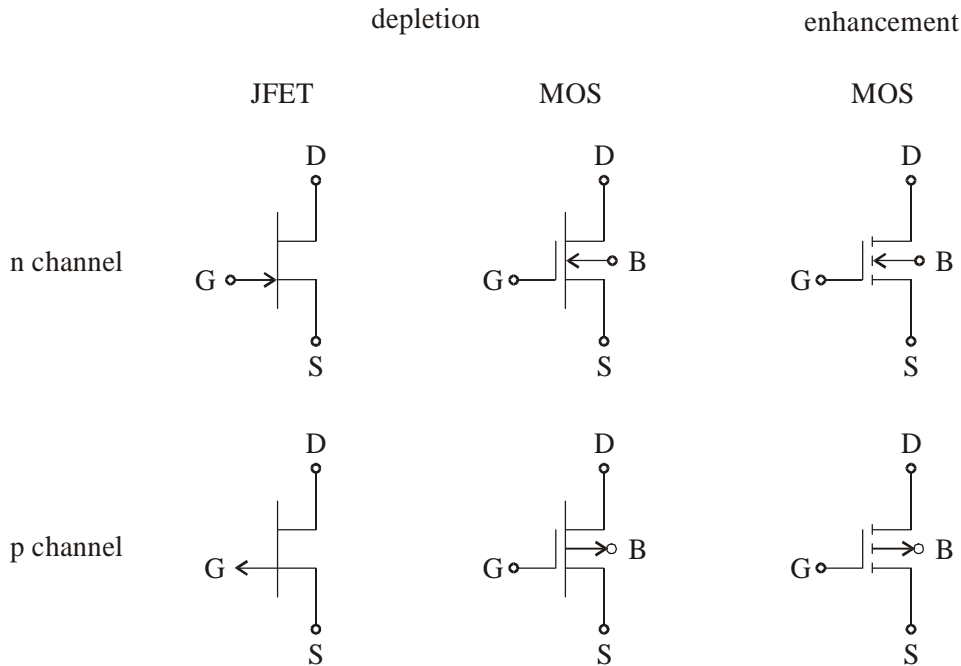
Power limits  $V_{DS} \cdot i_D < P_{D, max}$  + max voltages

**FET Facts:**

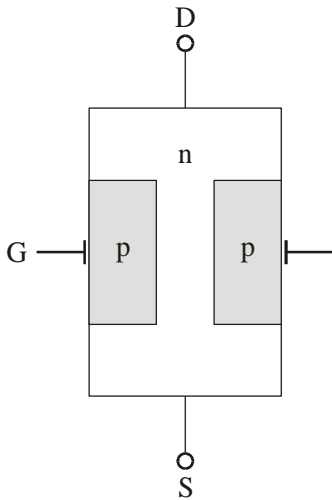
- 1) operation depends only on majority carrier flow  $\Rightarrow$  unipolar, (not bipolar like transistor)
- 2) more compact to fabricate  $\Rightarrow$  high packing density on Si
- 3) can function as a resistor  $\Rightarrow$  no other components needed for digital circuits
- 4) hi input impedance

**Disadvantages:**

- noisy at low frequencies
- lower speed than transistor, generally
- lower transconductance



JFET Large Signal Characteristics



Note this device technically inferior to MOSFET – the p-n junction is reverse biased for operation  $\Rightarrow$  leakage current  $G \rightarrow D$  is  $\sim 10^{-9}$  A, but is  $\sim 0$  for MOSFET since gate is insulated.  
 MOSFETs easy to destroy by static discharge  $\Rightarrow$  you'll use JFET in lab. (insulating layer gets 'punched through')  
 Also, p-n junction  $\Rightarrow$  strong temperature dependence!

On JFET: If a voltage  $v_{ds}$  is applied between drain & source, current  $i_D$  flows for  $v_{gs} = 0$ .

If we lower  $v_{gs} \Rightarrow$  electrons repelled from channel  $\Rightarrow$  less current flows.

Negative  $v_{gs}$  said to deplete the channel of charge carriers.

$v_{gs}$  negative enough  $\Rightarrow$  channel depleted & you 'pinch off' the channel. (see Sedra 5.11 for drawings & discussion)

For positive  $v_{gs}$ , gate-channel pn junction forward biased & gate can't control the channel  $\Rightarrow$  0V is maximum  $v_{gs}$  for JFET (n-channel)

I-V characteristics: similar to MOSFET depletion devices. Parameters of device specified in terms of pinch-off voltage  $V_P$  & drain-source current with gate shorted to the source  $I_{DSS}$ .

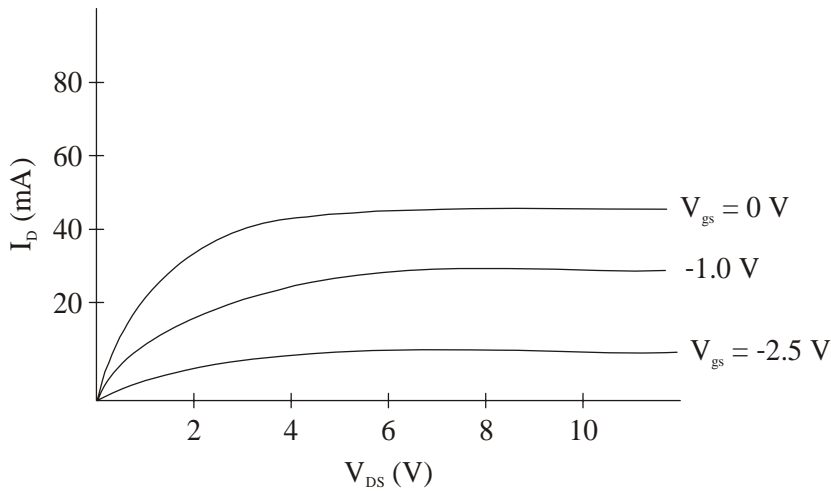
Operating regions: (n-channel)

1) cutoff:  $v_{gs} \leq V_P; i_D = 0$

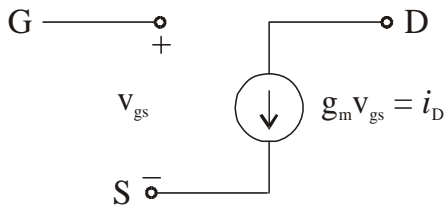
2) 'triode' region  $V_P \leq v_{gs} \leq 0 \quad v_{DS} \leq v_{gs} - V_P; \quad i_D = I_{DSS} \left[ 2 \left( 1 - \frac{v_{gs}}{V_P} \right) \left( \frac{v_{DS}}{-V_P} \right) - \left( \frac{v_{DS}}{V_P} \right)^2 \right]$

3) 'saturation' (pinch-off) region:  $V_P \leq v_{gs} \leq 0; \quad v_{DS} \geq v_{gs} - V_P; \quad i_D = I_{DSS} \left( 1 - \frac{v_{gs}}{V_P} \right)^2 \left( 1 + \frac{v_{DS}}{V_A} \right)$

$V_A \equiv$  'Early Voltage'  $\sim 100V \Rightarrow$  ignore      e.g.  $I_{DSS} = 50 \text{ mA} \quad V_P \sim -4V$



JFET Small Signal Model



Voltage-controlled current source

$$i_D = g_m v_{gs} \quad (1) \quad g_m \equiv \text{transconductance} \quad g_m = i_d / v_{gs} \Rightarrow \text{units of conductivity}$$

JFET is a voltage-operated device

$$g_m = \frac{\partial i_D}{\partial v_{gs}} \text{ from (1), so in saturation region, } i_D \approx I_{DSS} \left(1 - \frac{v_{gs}}{V_P}\right)^2 \text{ \&}$$

$$g_m = \frac{\partial i_D}{\partial v_{gs}} = -2I_{DSS} \left(1 - \frac{v_{gs}}{V_P}\right) * \left(\frac{1}{V_P}\right) \text{ (@ } v_{gs} \sim 1V, \sim 750\text{mA/V for } g_m)$$

Independent of  $v_{DS}$ , linear in  $v_{gs}$ !

NOTE:  $g_m$ ,  $V_P$ , etc. depend on physical device characteristics. Look at data sheets – also capacitances associated with junction, etc.

In ‘triode’ region

$$g_m = \frac{\partial}{\partial v_{gs}} \left\{ I_{DSS} \left[ 2 \left(1 - \frac{v_{gs}}{V_P}\right) \left(\frac{v_{DS}}{-V_P}\right) - \left(\frac{v_{DS}}{V_P}\right)^2 \right] \right\}$$

$$g_m = 2I_{DSS} \left(\frac{v_{DS}}{V_P^2}\right) \text{ dependent upon } v_{DS}!$$

Device Variation

FET characteristics (parameters) show much greater spread with FAB process than e.g. BJT, e.g. spread in  $V_P$  may be  $-0.5$  to  $-3V$  on sample devices from same batch.

⇒ Most design circuits to get around device variation to make circuits with predictable characteristics!

Various methods can be used in device layout to ‘match’ characteristics -  
 ‘interleaving’ channels so thermal & FAB effects cancel -  
 problem in obtaining uniform channel  
 doping over large areas & sensitive thermal dependence.

This is why people use bipolar for precision circuits.

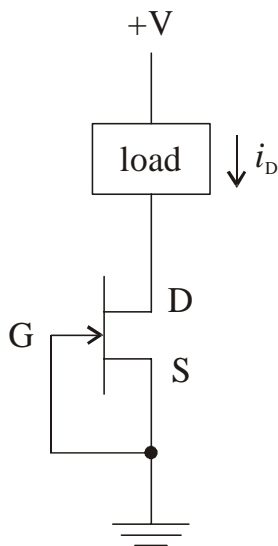
**Concept**

**Feedback**

- The best way to get around device variation is through the use of feedback.  
 feedback ≡ compare output of the system with the desired output to generate a control signal to input  
 e.g. you get bad HW grades, you do better next time
- Negative feedback ⇒ couple some output back so as to cancel input.
- At first, sounds stupid, but negative feedback improves circuit characteristics:  
 e.g. very high gain amplifier, ( $\times 10^6$ ) with strong negative feedback will have characteristics that depend on the property of the feedback elements only (we’ll see this later)
- Note also ‘negative’ ⇒  $180^\circ$  phase shift, between input & output!
- Positive feedback also possible – leads to oscillations  
 unwanted positive feedback – ‘parasitic’ oscillations  $\omega$  dependent due to stray caps in circuit!

**Circuit Analysis**

JFET Current Sources – Simplest example:



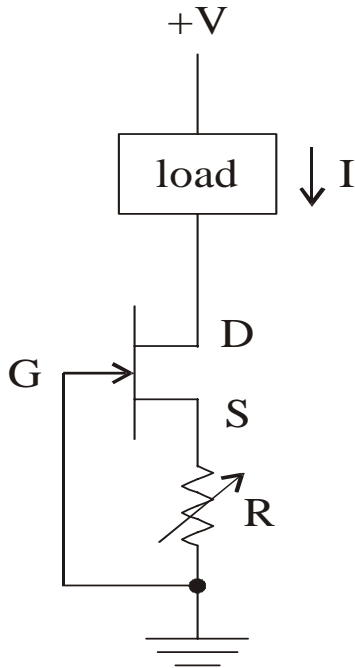
From I-V characteristics,  $i_D$  reasonably constant for  $v_{gs} = 0$ , for  $v_{DS} > 3V$ .

So, JFET looks like a current source.

However,  $I_{DSS}$  varies from device to device ⇒ value of  $i_D$  not predictable.

So it is a pretty good current source, but we don’t know the current!

- A variation gives an adjustable current source:



R is a 'self-biasing' resistor – back bias gate by  $I_D R$  & brings JFET closer to pinch-off, lowers  $i_{\text{drain}}$ .

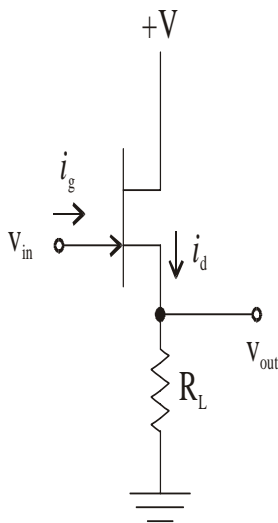
A form of current-sensing feedback.

Still some variation of output current with voltage  
( $\sim 2\%$  I vs. V variation)  $\Rightarrow$  not ideal

Vary R with each device to set  $i_{\text{drain}} (< I_{\text{DSS}})$

### Source Follower

Take advantage of high input impedance of JFET –  $i_g \approx 0$



We'll have

$$v_{\text{out}} = R_L i_D$$

$$i_g \sim 0$$

$$\text{but } i_d = g_m v_{gs} = g_m (v_{\text{in}} - v_{\text{out}})$$

So  $v_{\text{out}} = R_L g_m (v_{\text{in}} - v_{\text{out}})$  solve for  $v_{\text{out}} \Rightarrow$

$$\text{or } v_{\text{out}} = \frac{R_L g_m}{1 + R_L g_m} v_{\text{in}}$$

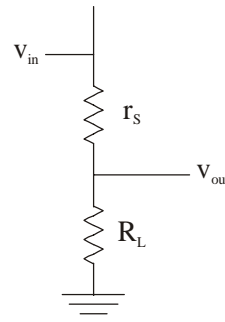
For  $R_L \gg \frac{1}{g_m}$ ,  $v_{\text{in}} \approx v_{\text{out}}$  (hence, follower) with very, very high input impedance!

Use to isolate sub circuit components.

NB: define  $r_s = 1/g_m \Rightarrow$

$$v_{out} = \frac{R_L}{r_s + R_L} v_{in} \text{ \& equivalent circuit looks like}$$

\& device behaves to keep  $v_{in} \approx v_{out}$  within  $r_s$ .



$\Rightarrow$  source-resistance model:

