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Advice:

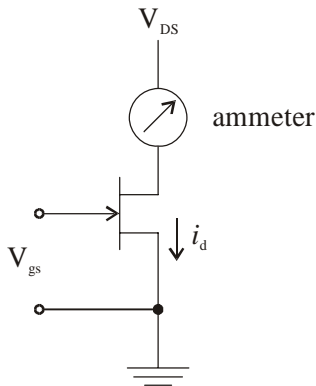
Today: lec 6 JFET II
 lec 7 TH Feb 15
 lec 8 TH Feb 22
 lec 9 TH Mar 8

Labs 1 & 2 solutions posted in hall.

Measurements

- How do we find JFET I_{drain} vs. V_{DS} characterization?

Logically:



Allows you to get v_{gs} , then vary V_{DS} while measuring current through JFET.

- We'll do something similar in the lab – measure v_{gs} vs. i_D .
- To get i_D vs. V_{DS} for various v_{gs} , use curve tracer.
- Similar tracers very useful for diodes, bipolar, etc
- In general, devices fabricated in a particular process have to be characterized, parameters extracted, and used in modeling behavior of the devices.
- This is a big industry – we engage in at lab in addition modeling radiation-damaged devices.

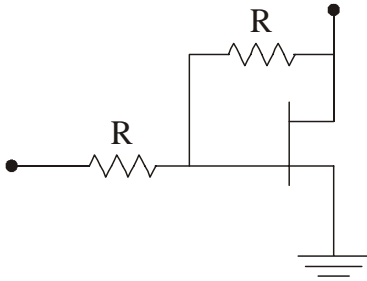
Instruments & Devices

- FETs can also act as resistors \Rightarrow for VLSI circuit FAB, very important – make caps out of silicon layers with SiO_2 between, resistors & transistors from FET.
- How is a JFET a resistor? For small signals, looks like a voltage-controller resistor. Look in 'triode' region, find $i_D / v_{DS} \Rightarrow$

From last time, $i_D = I_{DSS} \left[2 \left(1 - \frac{v_{gs}}{V_P} \right) \left(\frac{v_{DS}}{-V_P} \right) - \left(\frac{v_{DS}}{V_P} \right)^2 \right]$

Divide through by $v_{DS} \Rightarrow \frac{i_D}{v_{DS}} = \frac{1}{R_{DS}} = \frac{2I_{DSS}}{V_P^2} \left[(v_{gs} - V_P) - \frac{v_{DS}}{2} \right]$

- Second term is nonlinear – R depends on v, but for small $v_{DS} \approx 0$ & we get a pretty good resistor out of this.
- Extend the range of linearity by adding a signal to the gate of $v_{DS}/2 \Rightarrow$

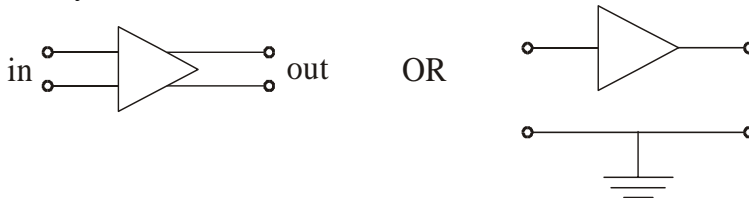


Handy – you check – $R_{DS} \sim \frac{1}{g_m}$. So resistance in linear region is the inverse of the transconductance in the saturated region.

Concept

Voltage Amplifier

- Generalize source follower discussion from last time
- Use symbol



For an amplifier:

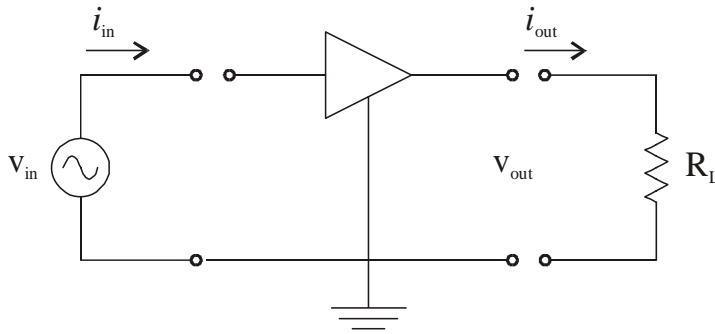
Accepts signal v_{in} and generates output v_{out}

Across a load R_L , where v_{out} is a magnified or (de-magnified) copy of v_{in}

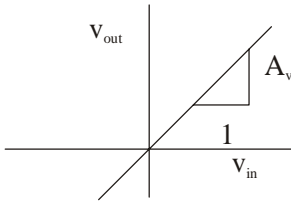
(Linear amp \Rightarrow amplitude & phase shift are only changes in v_{out} , no ω change.

-

- Voltage gain defined by voltage gain $A_v \equiv \frac{v_{out}}{v_{in}}$ (express in dB)



- Transfer characteristic is v_{out} vs. v_{in} :



- Voltage amps have power gain (contrast: transformer)

e.g. power gain $(A_p) = \frac{\text{load power } (P_L)}{\text{input power } (P_I)}$

$$= \frac{v_o i_o}{v_{in} i_{in}}$$

- So, JFET source follower last time has power gain $\approx \infty$ because i_{in} is 10^{-9} Amps
 i_{out} is mA
 so ratio $\approx 10^{12}$

- Likewise, current gain $A_i = \frac{i_o}{i_{in}}$ so $A_p = A_v A_i$
 (Extra power comes from the power supply!)

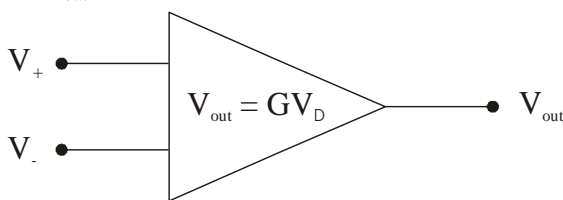
Concept

Differential Amplifiers – special version of amp

- 2 inputs & output ideally depends only on the difference between the 2 inputs

$$V_{\Delta} = \frac{(V_+ - V_-)}{2}$$

$\Rightarrow V_{out} = G V_{\Delta}$ where G is the gain of the differential amp.



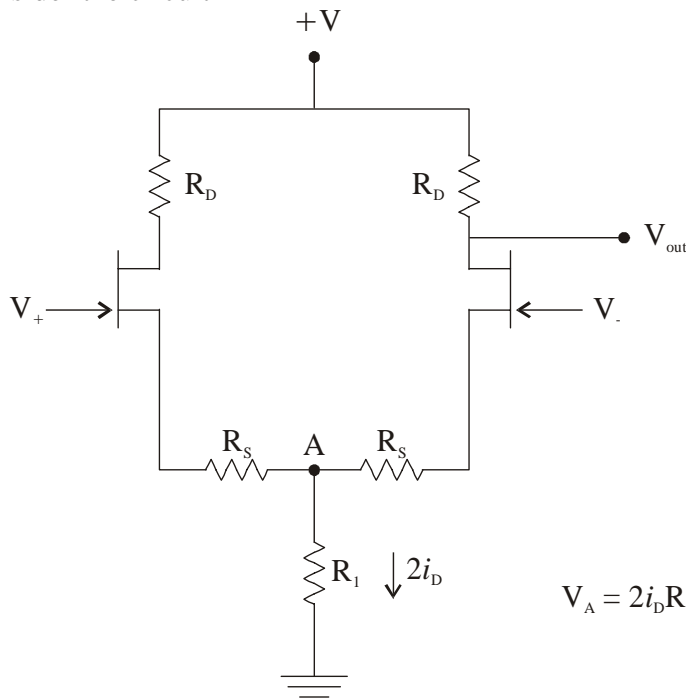
- Real differential amp depends on the average of the two input signals,

$$V_{\text{common mode}} \equiv V_c = \frac{(V_+ + V_-)}{2}$$

$$\Rightarrow \text{common mode gain} \equiv G_{\text{cm}} \ll G$$
- Used very commonly in analog circuits to reduce noise at the input – rejects signals ‘in common’ at 2 inputs, only ‘sees’ the difference.
- Constructed using a ‘matched pair’ of transistors – ideally, a pair with identical characteristics.

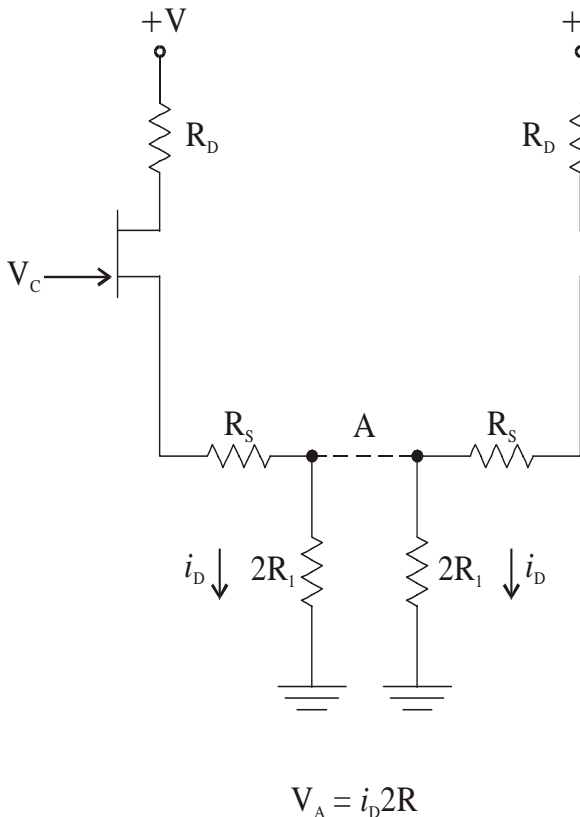
Circuit Analysis: Common Mode Gain

Discussed in notes, but important, so I’ll repeat.
 Consider the circuit



For common mode gain, $V_+ = V_- = V_c$

Redraw circuit as



Identical transistors, V_C same on both sides \Rightarrow both halves of circuit behave the same.

R_1 splits into 2 resistors of twice the original value ($V_A = i_D 2R$)

We'll have, using the source-resistance model

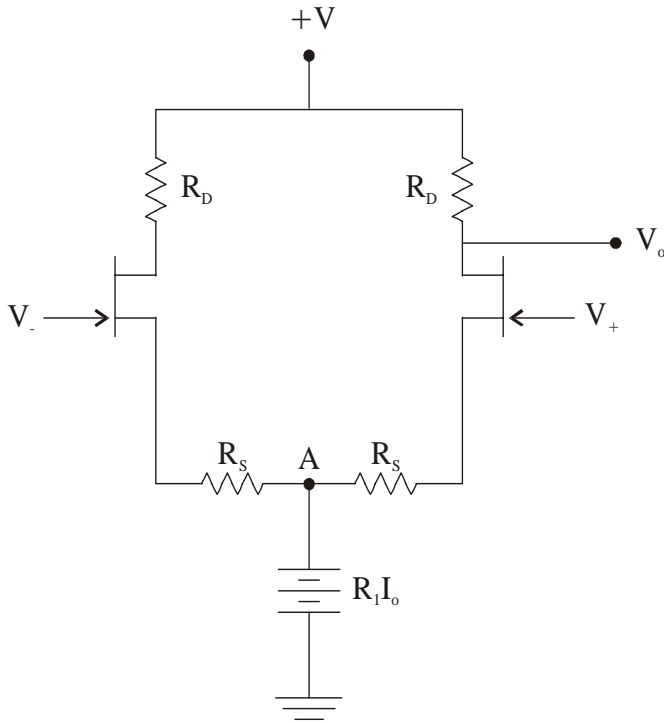
$$v_{out} = \frac{R_D v_C}{(2R_1 + R_S + r_s)} \quad r_s = 1/g_m$$

$$G_{cm} = \frac{v_{out}}{v_C} = \frac{R_D}{(2R_1 + R_S + r_s)}$$

$$R_1 \gg R_D \Rightarrow G_{cm} \approx 0$$

Circuit Analysis: Differential Gain

Response to differential signal V_D will be equal & opposite DC current flow (I_o) through $R_1 \Rightarrow$ voltage at point A will not change \Rightarrow Replace common resistor by voltage source of strength $R_1 I_o$:



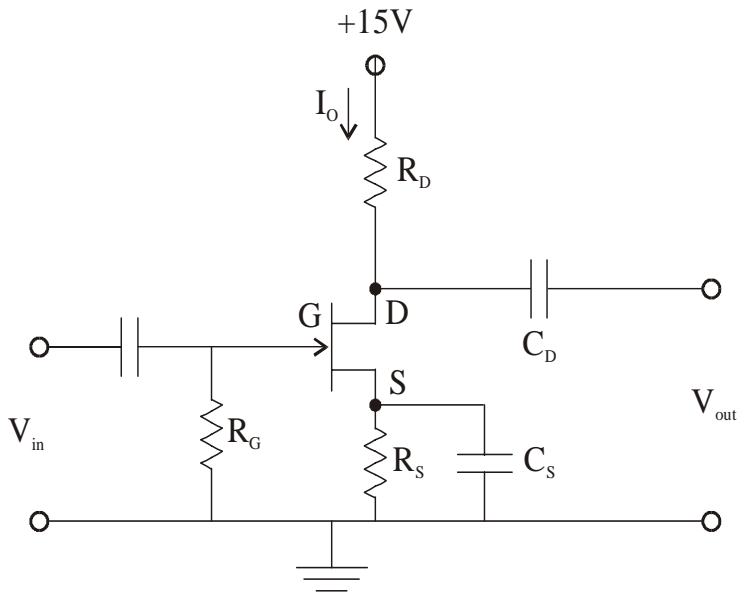
Again, use source-resistance model \Rightarrow

$$v_{out} = \frac{R_D V_{\Delta}}{R_S + r_s}$$

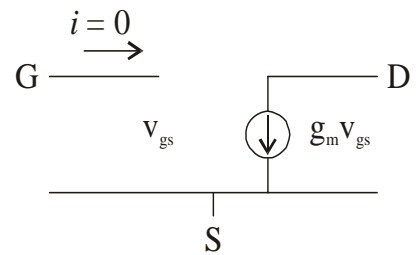
$$\text{So } G = \frac{V_{out}}{V_{\Delta}} = \frac{R_D}{R_S + r_s}$$

So, for $R_D \gg R_S$, gain is large

JFET Common Source Amplifier



small signal model:



Want $I_D \sim 5 \text{ mA}$

\Rightarrow look on characteristics (typical): $V_{DS} \sim 10\text{V}$ with $V_{gs} \sim -1.5\text{V} \Rightarrow g_m \sim 4 \times 10^{-3} \text{ 1}/\Omega$

No current flowing into the input \Rightarrow

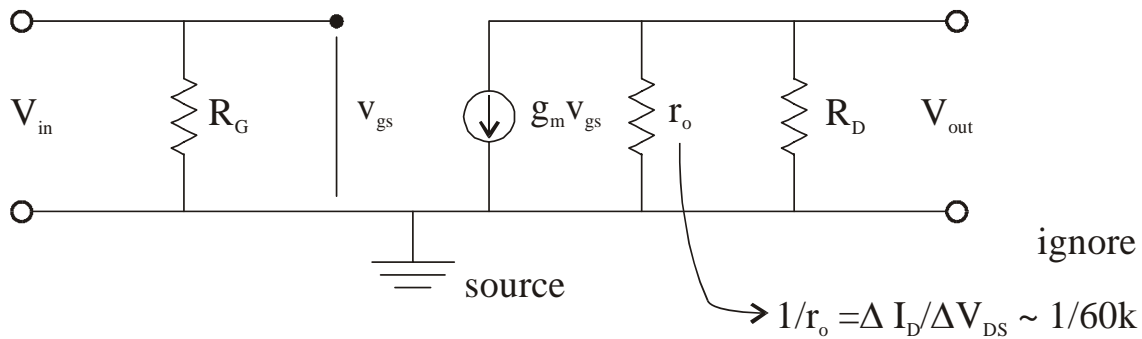
$$V_{GS} + V_S = 0 \Rightarrow V_{gs} = -1.5\text{V} = -V_S, \text{ or } V_S = 1.5\text{V}$$

$$\Rightarrow R_s = \frac{V_s}{I_D} = \frac{1.5V}{5mA} = 300\Omega$$

$$R_D = \frac{15V - 11.5V}{5mA} = \frac{3.5V}{5mA} \sim 700\Omega$$

Take R_G big $\Rightarrow R_G \sim 1m\Omega$

Small signal model: $(R_s C_s)^{-1} \sim 20Hz$, R_s out for high $v \Rightarrow$



Input impedance = $R_G = 1m\Omega$

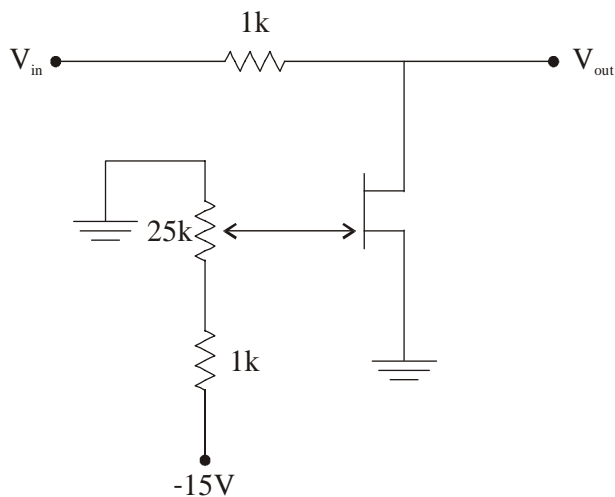
Output impedance = r_o in parallel with $R_D \sim R_D$

(small signal)

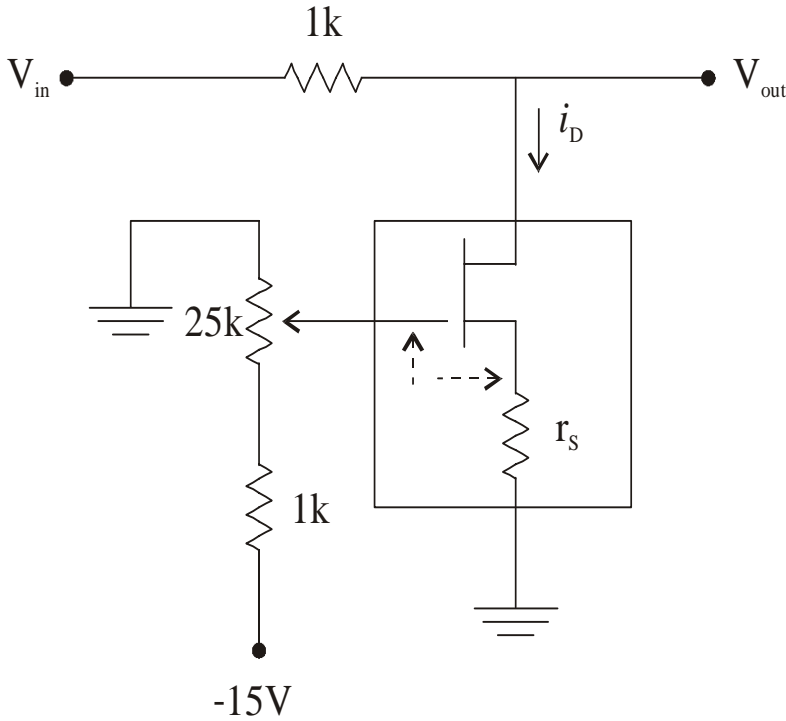
$$\begin{aligned} \text{gain} &= \frac{v_{out}}{v_{in}} = -\frac{(g_m v_{in})R_D}{v_{in}} = -g_m R_D \\ &= -\left(4 \times 10^{-3} \frac{1}{\Omega}\right)(700\Omega) \sim -3 \end{aligned}$$

Circuit Analysis

JFET Attenuator



Use small signal source resistance model for the JFET:

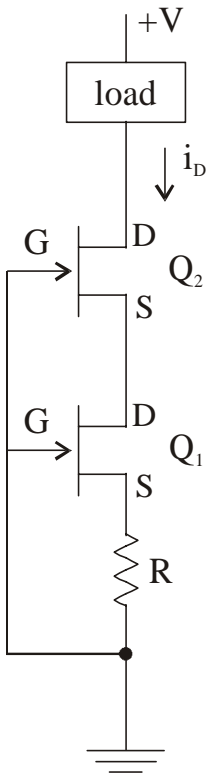


$$\Rightarrow V_{out} = i_D \cdot r_S$$

$$V_{out} = \frac{V_{in} \cdot r_S}{1k + r_S}$$

You'll improve linearity range of this in the lab.

A smarter circuit: 'CASCODE'



Idea: use second JFET (Q_1) to hold constant the drain-source voltage v_{DS} of the current source.

Q_2 passes Q_1 's constant drain current through the load, while holding Q_1 's drain at fixed voltage – namely, the v_{gs} that makes Q_2 operate at the same current as Q_1

$\Rightarrow Q_2$ shields Q_1 from voltage swings at the drain

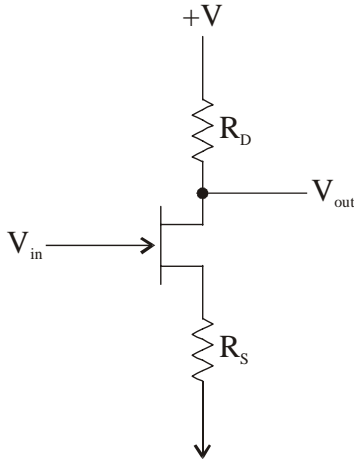
$\Rightarrow Q_1$ just sits there & makes a constant current

For this to work, max current of Q_2 (I_{DSS}) must be larger than I_{DSS} of Q_1 – have to be able to keep both transistors 'on'!

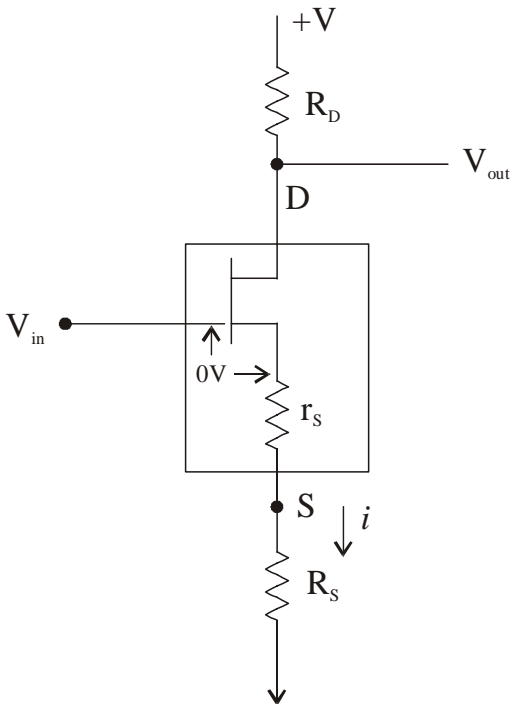
Circuit Example from Lab 6 Notes

(important, so I point out)

Voltage Amplifier



Use source-resistance small signal model



Note $i = \frac{v_{in}}{R_S + r_s}$ (0V G-S voltage)

$$r_s = 1/g_m$$

We don't care about R_D for this

so $v_{out} = -R_D i$ (as if R_D goes to ground)

$$= -\frac{R_D}{R_S + r_s} v_{in}$$

So $gain = v_{out}/v_{in} \cong -\frac{R_D}{R_S}$ ($R_S \gg r_s$)